18.3 A 45nm Low-Standby-Power Embedded SRAM with Improved Immunity Against Process and Temperature Variations

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Embedded SRAM in sub-50nm advanced CMOS technology is facing the crisis of increasing threshold voltage (V_t) variation [1]. In particular, the random V_t variation caused by dopant fluctuation degrades the SRAM operating margin. We propose SRAM read/write assist circuits to enlarge the operating margin against wide process and temperature variations with a single supply voltage in the 45nm low standby power LSTP technology.

The SRAM read margin is represented by the static noise margin (SNM), and is improved by lowering the voltage level of the word-line (WL). Figure 18.3.1 shows the read assist circuit (RAC) to control the WL voltage (V_{WL}). In conventional circuitry [2], V_{WL} is lowered by mutliple pull-down NMOS transistors (called replica access transistors, RATs), and depends on the V_t of the RAT (V_{tn}) and that of the logic transistor P0 (V_{tp}) in the WL driver. According to the simulated results of V_{WL} versus V_t plot for two temperatures, there are two problems in the conventional circuit (see dotted line in Fig. 18.3.1). The first problem is the V_{WL} in the fast NMOS, slow PMOS (FS) condition drops too much at –40°C, which degrades the cell current (or the operating speed) and the write margin. This degradation strongly depends on the temperature dependence of mobility and the V_t of SRAM RAT and logic P0. The second problem is a decrease in the V_{WL} at the slow NMOS, slow PMOS (SS) condition. From the simulation results in Fig. 18.3.1, V_{WL} at SS, which is the worst condition of the cell current, is lower than that at typical NMOS, typical PMOS (TT) due to the higher V_{tp}, resulting in a further degradation of the cell current. The proposed circuitry is designed to overcome these problems. The RATs are introduced to the source of the WL driver with additional passive resistance elements (R) implemented using N^+ polysilicon gate. The VA of WL driver's V_{DD} level (which is equivalent to V_{WL}) is determined by the ratio between the resistance R and the RATs (see solid lines in Fig. 18.3.1). Furthermore, since the gate length in the SS condition becomes longer due to process variations, we can expect a lower R value at SS. Therefore, the V_{WL} is kept at a high voltage level, leading to no loss of cell current which appears in [2]. In addition, as the temperature dependence of a resistance element is generally smaller than that of MOS transistors, we can also suppress the temperature dependence on V_{WL}.

Figure 18.3.2 shows the implemented RAC with the gate controller for the RAT. Due to the narrow gate width in the SS condition, a lower VB voltage is expected by the R1 of larger resistance. Because of the process dependence of the VB, the V_{WL} is kept at a higher voltage in the SS condition compared with the case using pull-down NMOS. In order to reflect the process variation of the gate length L and width W of the access transistor, the line width of polysilicon (R0, R2) and the diffusion elements (R1) have the same size as L and W, respectively. In addition, the polysilicon pitch of R0 and R2 is equal to that of the SRAM cell. Figure 18.3.2 also shows the simulated waveforms focusing on WL activation. The RAC does not affect the rising operation of the WL voltage.

Figure 18.3.3 shows the write-assist circuit (WAC). Lowering the supply voltage in the memory cell array (ary-VDM) is one effective way of ensuring the SRAM write margin [2,3]. The capacitive WAC makes use of the capacitance ratio between the ary-VDM (Cav) and the additional dmy-VDM (Cdv) [2]. To enhance the write margin against the increasing variation accompanied by the scaling, it is necessary to lower the voltage of ary-VDM (V_{AV}), which requires a small Cav/Cdv. If the Cdv is enlarged, it degrades the speed and power of the writing operation. Therefore, we propose a divided ary-VDM scheme. According to V_t curve simulation [4], the V_{AV} should be reduced by about 30% from V_{DD}. In addition, our simulation indicates that this V_{AV} does not affect the data retention, so that we divided the ary-VDM into eight. In the write state, as one of the BL pair is forced low and the XH of upper decode signal is activated, the V_{AV} falls to the voltage level determined by Cav/Cdv.

Figure 18.3.4 shows the simulated waveforms in the read and write cycle in the fast condition and slow condition. The V_{WL} is from 8% to 30% lower than V_{DD} due to the application of the RAC during both the read and write cycles. During the write cycle, the lowered V_{AV} is achieved.

Figure 18.3.5 is a SEM photograph of a 6T SRAM memory cell array using our 45nm bulk CMOS technology with a SiON gate. The lithography of the critical dimension layers is utilized by the ArF immersion exposure technology. Two cell size were made: 0.327μm² and 0.245μm². The first cell was designed by considering a large V_t variation, and has a good functionality at 512Kbits. The second cell, which has the smallest feature size ever reported in the 45nm generation, was realized by taking the scaling trend into account. According to the measurement results, the SNM of the 0.327μm² cell without the RAC is 150mV, while that with the RAC is 214mV. Even the SNM of the 0.245μm² cell is 208mV using the RAC.

Figure 18.3.6 shows the measured relationship between the cell current and the SNM for several wafers with different V_t conditions. All the points indicate the mean values measured in each wafer. By introducing our RAC, it is confirmed that the SNM in the FS condition for both 0.245μm² and 0.327μm² cells increases by about 100mV. On the other hand, the cell current at SS in 0.327μm² with our RAC is twice as large as that with the conventional RAC. In addition, the cell current at FS is drastically improved in comparison with the conventional RAC. These improvements are the result of the V_{WL} dependence on the temperature (see Fig. 18.3.1) so that our RAC realizes stable read margin without the degradation of the operation speed for wide temperature region, which appeared in the conventional RAC. Another advantage is that the SNM and the cell current with RAC have smaller distributions against V_t change than those without RAC. This indicates that the SRAM with our proposed RAC has immunity against the large process variations. Figure 18.3.6 also shows the measured write margins [5]. In our circuitry, the write margin is affected not only by the WAC but also by the RAC. The lower write margin in the SF condition without an assist circuit is improved due to a dominant V_{AV} rather than V_{WL} (see Fig. 18.3.1). Though the write margin at the FS condition is suppressed by the V_{WL} lowering, it is kept higher than that at SF, so SF remains the worst condition. Compared with the case without assist circuits, the write margin was improved by about 50 mV. In this way, it is expected that the SRAM with cell size of both 0.327μm² and 0.245μm² will show the full functionality.

Figure 18.3.7 is a die micrograph of the 1Mb SRAM macro. It consists of two conventional 256Kb SRAM macros and two proposed 256Kb SRAM macros. The area size of later the 256Kb SRAM macro is 550×305μm². The area penalty of the read and write assist circuit is less than 10%.

References:

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[5] R. Heald and P. Wang, "Variability in Sub-100nm SRAM designs," *ICCAD* Digest, pp. 347-352, Nov., 2004.

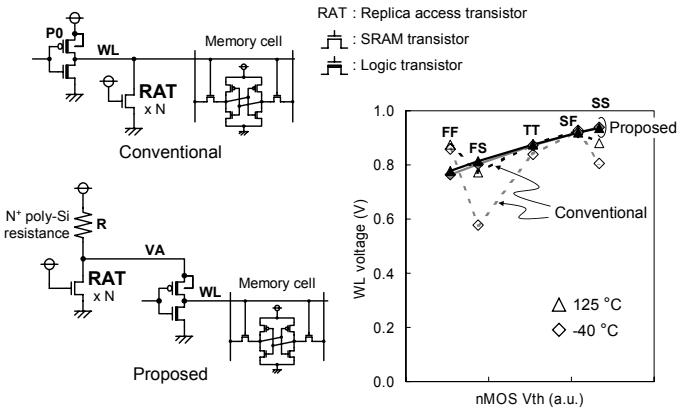

Figure 18.3.1: Concept of improving read stability depending on process and temperature variations.

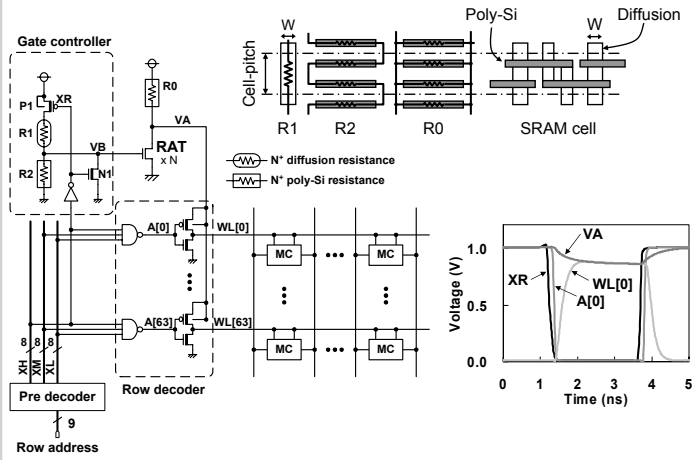

Figure 18.3.2: Practical read assist circuit (RAC).

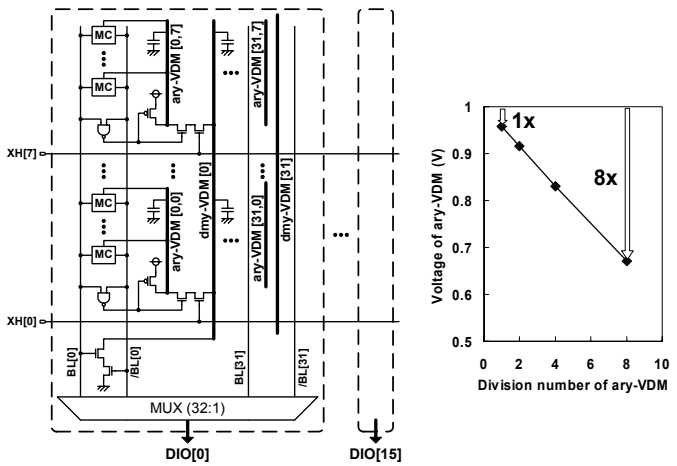

Figure 18.3.3: Write assist circuit (WAC) improving write stability.

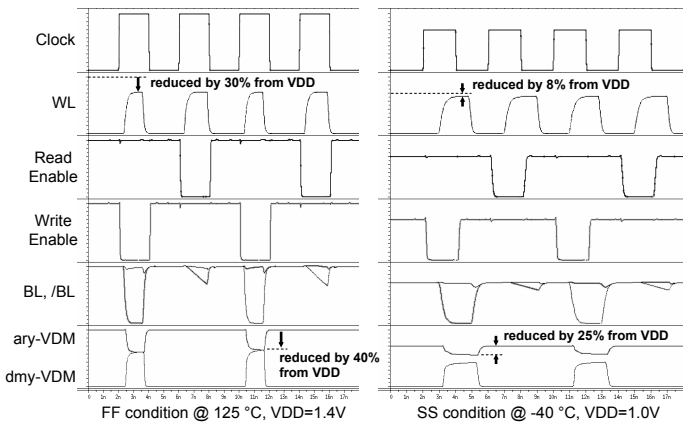

Figure 18.3.4: Simulated waveform of 512 Kbit SRAM macro.

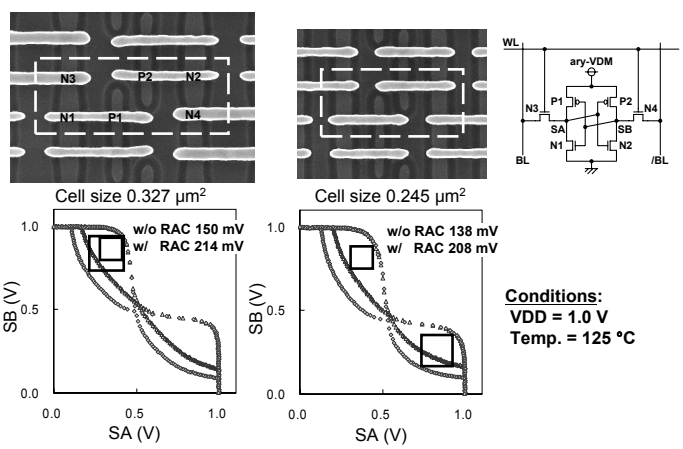

Figure 18.3.5: SEM photograph of 6T SRAM cell and measured SNM.

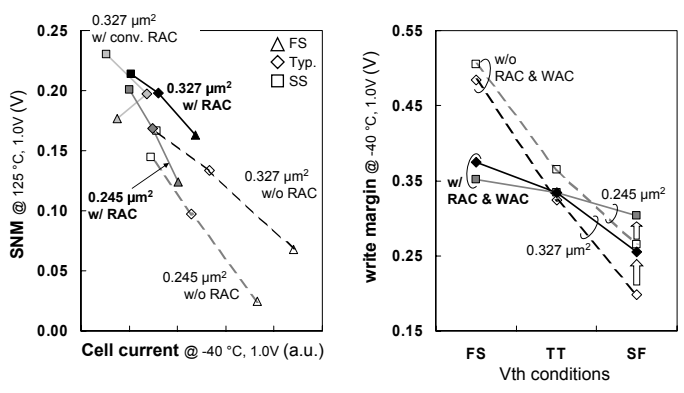

Figure 18.3.6: Measured DC characteristics of 6T SRAM cells at worst-case temperature.

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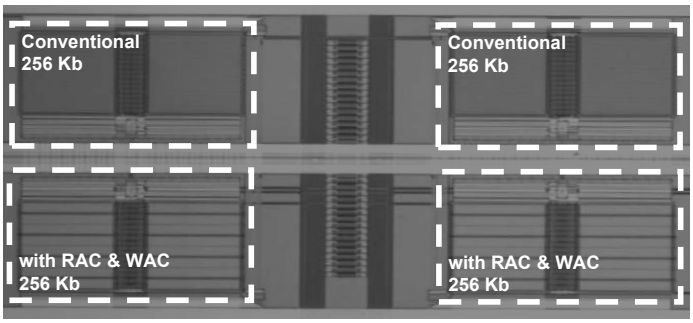

Figure 18.3.7: Die micrograph.

